



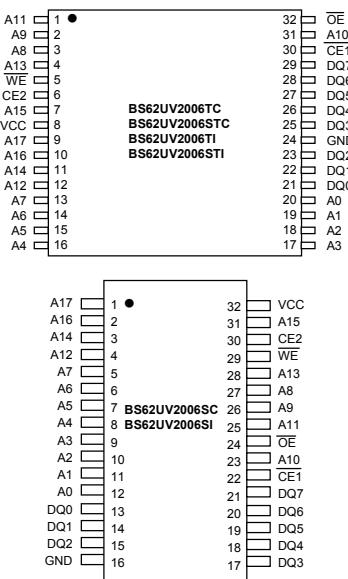
■ FEATURES

- Wide Vcc operation voltage :
 - C-grade: 1.8V~3.6V
 - I-grade: 1.9V~3.6V
 - (Vcc_min.=1.65V at 25°C)
- Ultra low power consumption :
 - Vcc = 2.0V C-grade : 8mA (Max.) operating current
 - I-grade : 10mA (Max.) operating current
 - 0.20uA (Typ.) CMOS standby current
 - Vcc = 3.0V C-grade : 11mA (Max.) operating current
 - I-grade : 13mA (Max.) operating current
 - 0.30uA (Typ.) CMOS standby current
- High speed access time :
 - 85 85ns (Max.)
 - 10 100ns (Max.)
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation

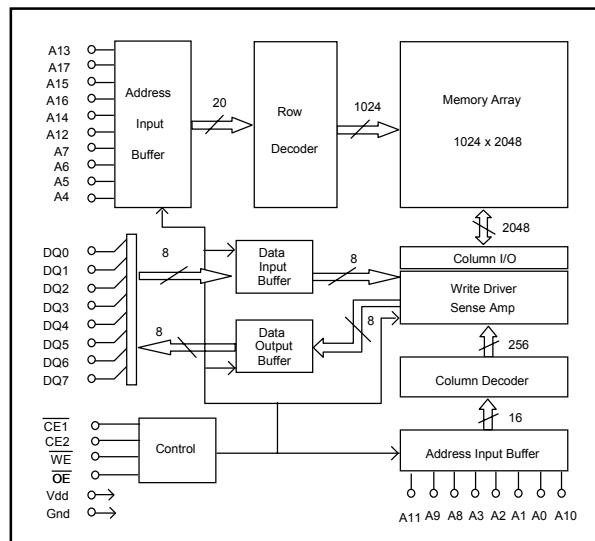
■ PRODUCT FAMILY

PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION				PKG TYPE
				STANDBY (ICCSB1, Max)		Operating (Icc, Max)		
BS62UV2006DC			C-grade:1.8~3.6V I-grade:1.9~3.6V	Vcc=3.0V	Vcc=2.0V	Vcc=3.0V	Vcc=2.0V	DICE
BS62UV2006TC	+0°C to +70°C	1.8V ~ 3.6V	85/100	3.0uA	2.0uA	11mA	8mA	TSOP-32
BS62UV2006STC								STSOP-32
BS62UV2006SC								SOP-32
BS62UV2006DI								DICE
BS62UV2006TI								TSOP-32
BS62UV2006STI	-40°C to +85°C	1.9V ~ 3.6V	85/100	5.0uA	3.0uA	13mA	10mA	STSOP-32
BS62UV2006SI								SOP-32

■ PIN CONFIGURATIONS



■ BLOCK DIAGRAM



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■ PIN DESCRIPTIONS

Name	Function
A0-A17 Address Input	These 18 address inputs select one of the 262,144 x 8-bit words in the RAM
CE1 Chip Enable 1 Input CE2 Chip Enable 2 Input	CE1 is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
WE Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when WE is HIGH and OE is LOW, output data will be present on the DQ pins; when WE is LOW, the data present on the DQ pins will be written into the selected memory location.
OE Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when OE is inactive.
DQ0-DQ7 Data Input/Output Ports	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	WE	CE1	CE2	OE	I/O OPERATION	Vcc CURRENT
Not selected (Power Down)	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
	X	X	L	X		
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	DOUT	I_{CC}
Write	L	L	H	X	DIN	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	PARAMETER	RATING	UNITS
VTERM	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TBIAS	Temperature Under Bias	-40 to +85	°C
TSTG	Storage Temperature	-60 to +150	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0 °C to +70 °C	1.8V ~ 3.6V
Industrial	-40 °C to +85 °C	1.9V ~ 3.6V

■ CAPACITANCE⁽¹⁾ (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CDQ	Input/Output Capacitance	VI/O=0V	8	pF

1. This parameter is guaranteed and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = -40°C to + 85°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNITS	
V _{IL}	Guaranteed Input Low Voltage ⁽²⁾	Vcc=2.0V Vcc=3.0V	-0.3 ⁽⁵⁾	--	0.6	V	
V _{IL}	Guaranteed Input High Voltage ⁽²⁾		--	--	0.8		
V _{IH}	Guaranteed Input High Voltage ⁽²⁾	Vcc=2.0V Vcc=3.0V	1.4	--	Vcc+0.3	V	
V _{IH}	Guaranteed Input Low Voltage ⁽²⁾		2.0	--			
I _{IL}	Input Leakage Current	Vcc = Max, V _{IN} = 0V to Vcc	--	--	1	uA	
I _{IO}	Output Leakage Current	Vcc = Max, $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$, V _{IO} = 0V to Vcc	--	--	1	uA	
V _{OL}	Output Low Voltage	Vcc = Max, I _{OL} = 0.1mA Vcc = Max, I _{OL} = 2.0mA	Vcc=2.0V Vcc=3.0V	-- --	0.2 0.4	V	
V _{OH}	Output High Voltage	Vcc = Min, I _{OH} = -0.1mA Vcc = Min, I _{OH} = -1.0mA	Vcc=2.0V Vcc=3.0V	Vcc-0.2 2.4	-- --		
I _{CC}	Operating Power Supply Current	Vcc = Max, $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$ I _{DO} = 0mA, F = Fmax ⁽³⁾	Vcc=2.0V Vcc=3.0V	-- --	10 13	mA	
I _{CCSB}	Standby Current-TTL	Vcc = Max, CE1 = V _{ih} or CE2 = V _{il} I _{DO} = 0mA	Vcc=2.0V Vcc=3.0V	-- --	0.1 0.5		
I _{CCSB1} ⁽⁴⁾	Standby Current-CMOS	Vcc = Max, $\overline{CE1} \geq Vcc - 0.2V$ or $CE2 \leq 0.2V$; V _{IN} $\geq Vcc - 0.2V$ or V _{IN} $\leq 0.2V$	Vcc=2.0V Vcc=3.0V	-- --	0.20 0.30	3.0 5.0	uA

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.

3. Fmax = 1/t_{RC}. 4. Iccsb1 is 2.0uA/3.0uA at Vcc=2.0V/3.0V and TA=70°C. 5. V_{IL} = -1.5V for pulse width less than 30ns.

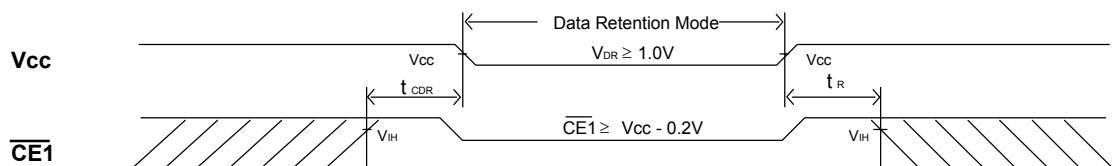
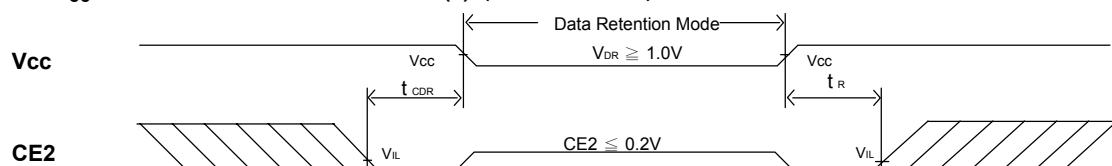
■ DATA RETENTION CHARACTERISTICS (TA = -40°C to + 85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNITS
V _{DR}	Vcc for Data Retention	$\overline{CE1} \geq Vcc - 0.2V$ or $CE2 \leq 0.2V$, V _{IN} $\geq Vcc - 0.2V$ or V _{IN} $\leq 0.2V$	1.0	--	--	V
I _{CCDR} ⁽³⁾	Data Retention Current	$\overline{CE1} \geq Vcc - 0.2V$ or $CE2 \leq 0.2V$, V _{IN} $\geq Vcc - 0.2V$ or V _{IN} $\leq 0.2V$	--	0.1	1.0	uA
t _{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t _R	Operation Recovery Time		T _{RC} ⁽²⁾	--	--	ns

1. Vcc = 1.0V, T_A = + 25°C

2. t_{RC} = Read Cycle Time

3. Iccdr is 0.7uA at TA=70°C.

■ LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)

■ LOW V_{CC} DATA RETENTION WAVEFORM (2) ($CE2$ Controlled)


■ AC TEST CONDITIONS

(Test Load and Input/Output Reference)

Input Pulse Levels	Vcc / 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5Vcc
Output Load	C _L = 100pF+1TTL C _L = 30pF+1TTL

■ KEY TO SWITCHING WAVEFORMS

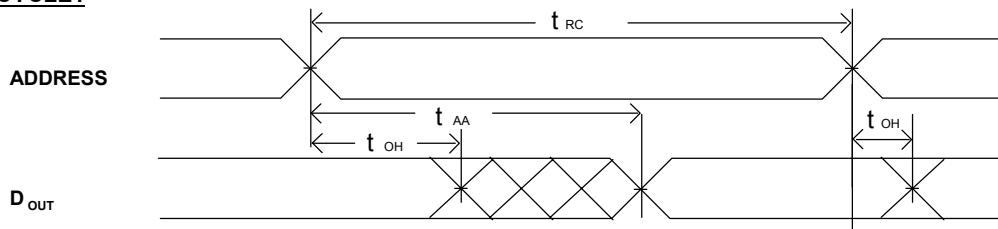
WAVEFORM	INPUTS	OUTPUTS
—	MUST BE STEADY	MUST BE STEADY
/ \ \ / \ \	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
/ \ \ / \ \	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
X X X X	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
X X X X	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

■ AC ELECTRICAL CHARACTERISTICS (TA = -40°C to + 85°C) READ CYCLE

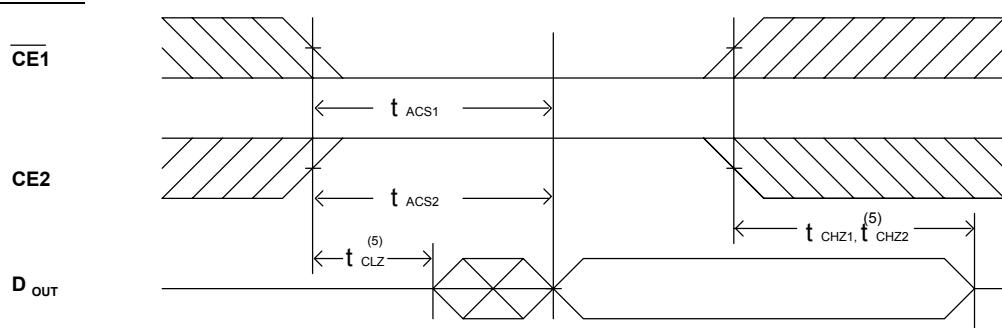
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 100ns (Vcc = 1.9-3.6V)			CYCLE TIME : 85ns (Vcc = 1.9-3.6V)			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t _{AVAX}	t _{RC}	Read Cycle Time	100	--	--	85	--	--	ns
t _{AVQV}	t _{AA}	Address Access Time	--	--	100	--	--	85	ns
t _{E1LQV}	t _{ACS1}	Chip Select Access Time (CE1)	--	--	100	--	--	85	ns
t _{E2HOV}	t _{ACS2}	Chip Select Access Time (CE2)	--	--	100	--	--	85	ns
t _{GLQV}	t _{OE}	Output Enable to Output Valid	--	--	45	--	--	40	ns
t _{E1LQX}	t _{CLZ1}	Chip Select to Output Low Z (CE1)	15	--	--	15	--	--	ns
t _{E2HQX}	t _{CLZ2}	Chip Select to Output Low Z (CE2)	15	--	--	15	--	--	ns
t _{GLQX}	t _{OLZ}	Output Enable to Output in Low Z	15	--	--	10	--	--	ns
t _{E1HQZ}	t _{CHZ1}	Chip Deselect to Output in High Z (CE1)	--	--	40	--	--	35	ns
t _{E2HQZ}	t _{CHZ2}	Chip Deselect to Output in High Z (CE2)	--	--	40	--	--	35	ns
t _{GHQZ}	t _{OHZ}	Output Disable to Output in High Z	--	--	35	--	--	30	ns
t _{AXOX}	t _{OH}	Data Hold from Address Change	15	--	--	15	--	--	ns

■ SWITCHING WAVEFORMS (READ CYCLE)

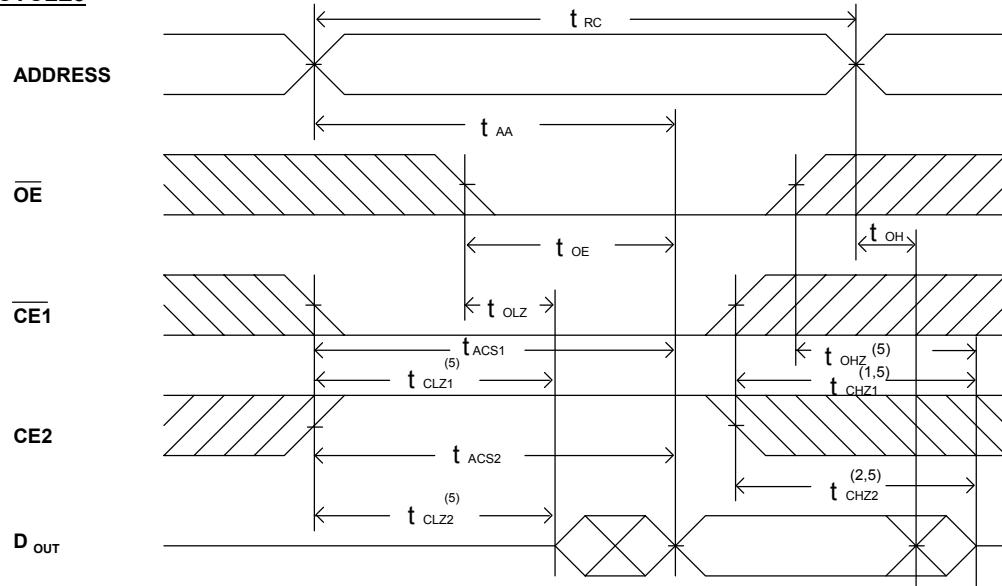
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)

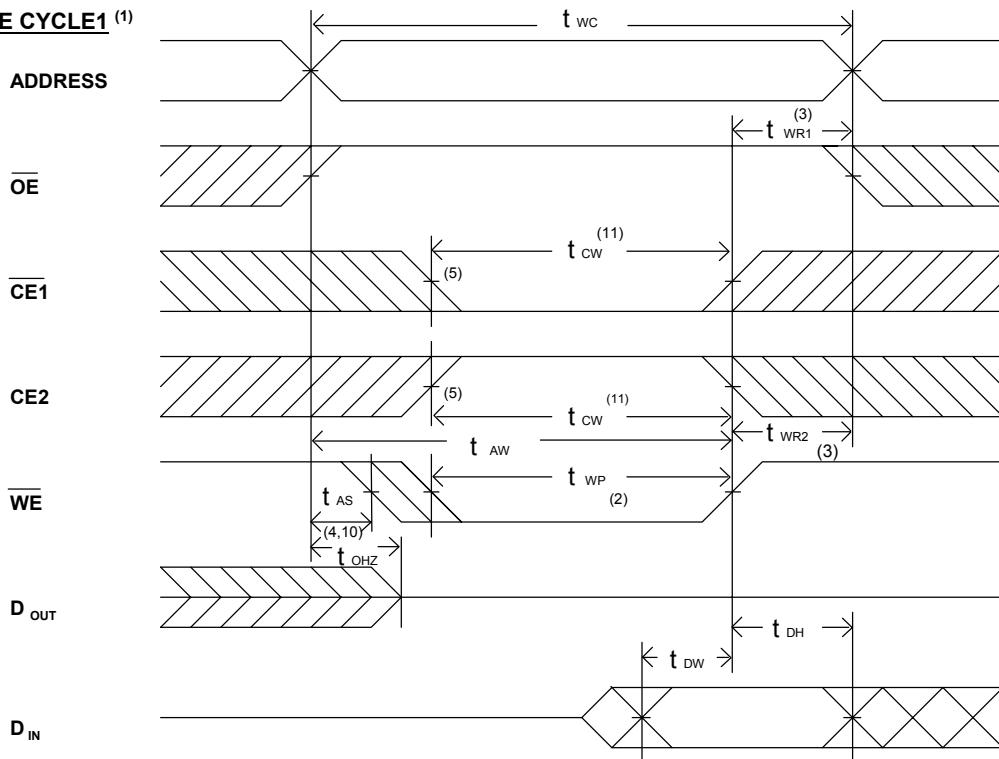


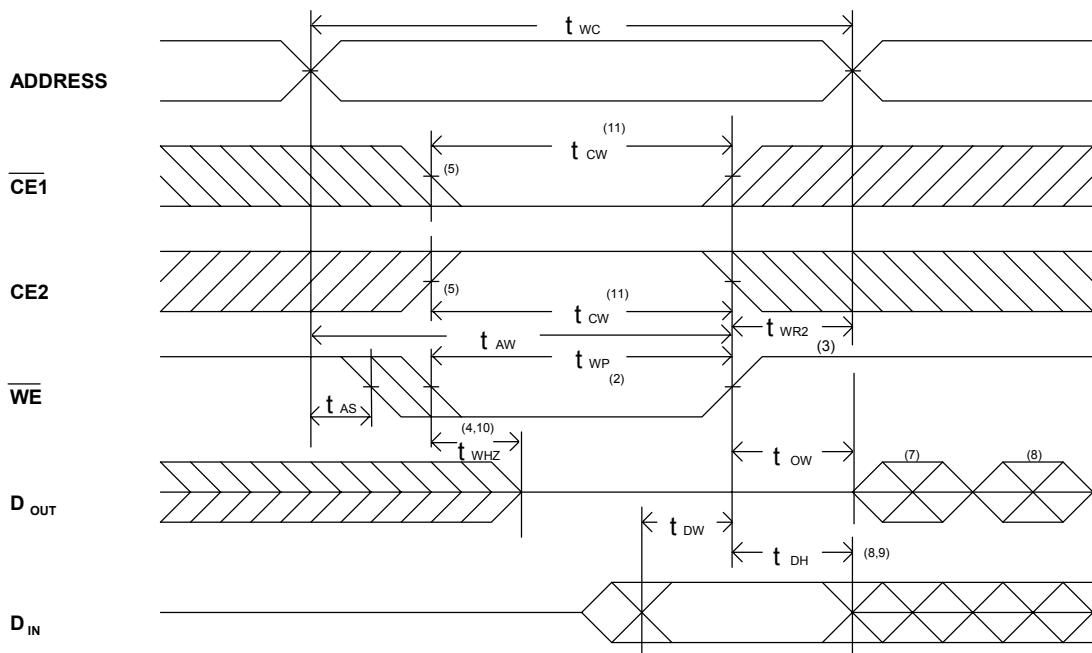
NOTES:

1. WE is high in read Cycle.
2. Device is continuously selected when $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and/or $CE2$ transition high.
4. $\overline{OE} = V_{IL}$.
5. The parameter is guaranteed but not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS (TA = -40°C to + 85°C)
WRITE CYCLE

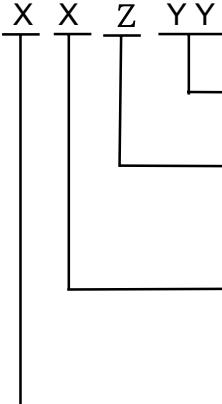
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 100ns (Vcc = 1.9~3.6V)			CYCLE TIME : 85ns (Vcc = 1.9~3.6V)			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	100	--	--	85	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	100	--	--	85	--	--	ns
t_{AVWL}	t_{AS}	Address Setup Time	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	100	--	--	85	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	--	--	40	--	--	ns
t_{WHAX}	t_{WR1}	Write recovery Time ($\overline{CE1}, \overline{WE}$)	0	--	--	0	--	--	ns
t_{E2LAX}	t_{WR2}	Write recovery Time ($CE2$)	0	--	--	0	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	--	--	40	--	--	35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	40	--	--	35	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	40	--	--	35	ns
t_{WHOX}	t_{ow}	End of Write to Output Active	10	--	--	10	--	--	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)
WRITE CYCLE1 ⁽¹⁾


WRITE CYCLE2 (1,6)

NOTES:

1. WE must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of CE1 and CE2 active and WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. TWR is measured from the earlier of CE1 or WE going high or CE2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CE1 low transition or the CE2 high transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.
6. OE is continuously low (OE = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CE1 is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of CE1 going low or CE2 going high to the end of write.

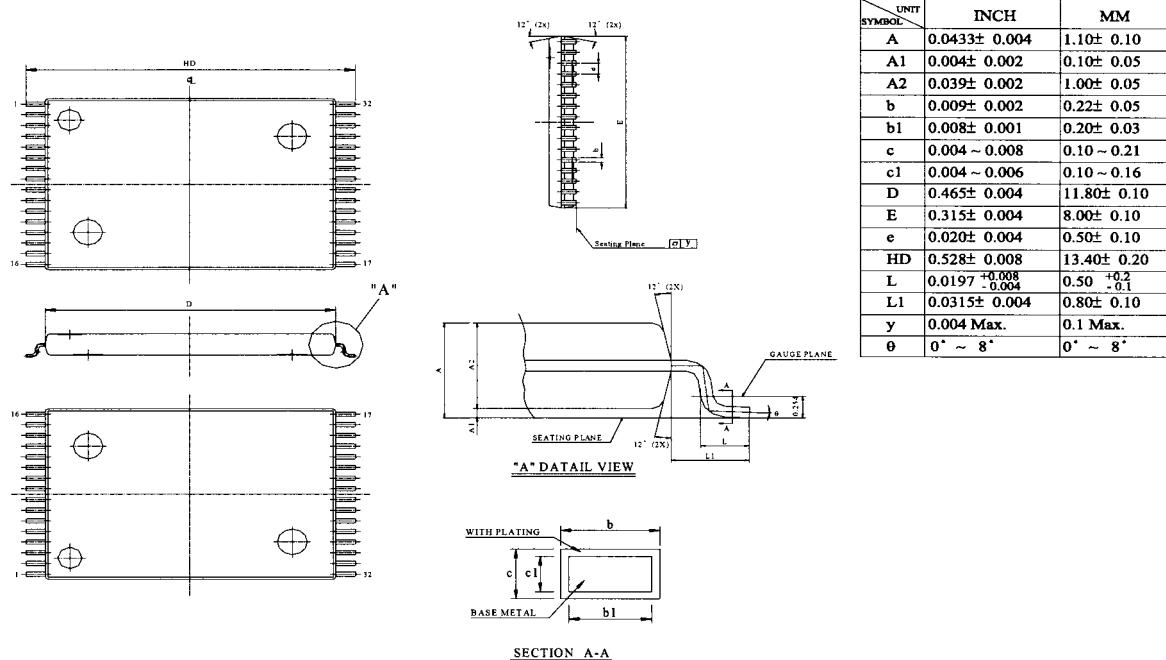
■ ORDERING INFORMATION

BS62UV2006 	SPEED 85: 85ns 10: 100ns
	PKG MATERIAL -: Normal G: Green P: Pb free
	GRADE C: +0°C ~ +70°C I: -40°C ~ +85°C
	PACKAGE S: SOP T: TSOP (8mm x 20mm) ST: Small TSOP (8mm x 13.4mm) D: DICE

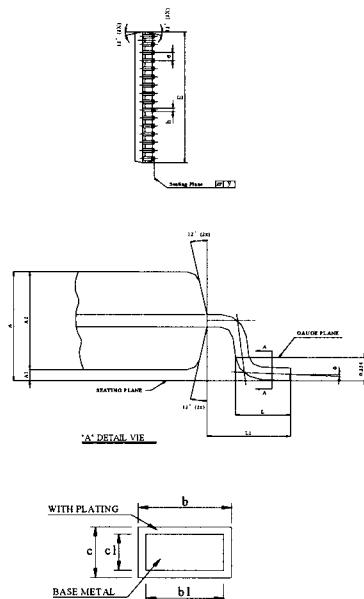
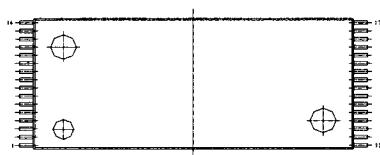
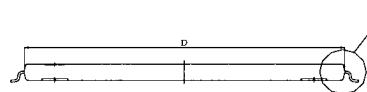
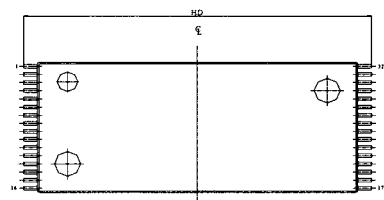
Note:

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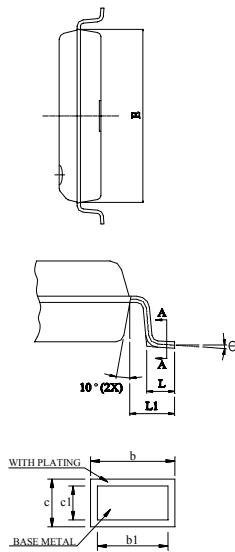
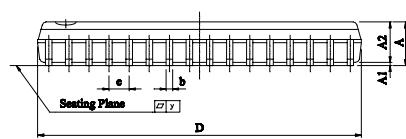
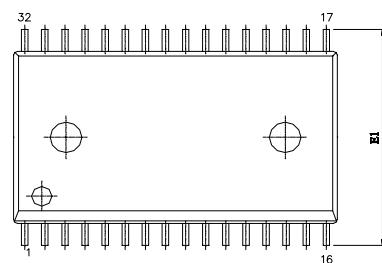
■ PACKAGE DIMENSIONS



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■ PACKAGE DIMENSIONS (continued)


UNIT SYMBOL	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.009± 0.002	0.22± 0.05
b1	0.008± 0.001	0.20± 0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.724± 0.004	18.40± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.020± 0.004	0.50± 0.10
HD	0.787± 0.008	20.00± 0.20
L	0.0197 ± 0.004	0.50 ± 0.1
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

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UNIT SYMBOL	INCH	MM
A	0.111±0.007	2.821±0.176
A1	0.009±0.005	0.229±0.127
A2	0.1055±0.0055	2.680±0.140
b	0.014 ~ 0.020	0.35 ~ 0.50
b1	0.014 ~ 0.018	0.35 ~ 0.46
c	0.006 ~ 0.012	0.15 ~ 0.32
c1	0.006 ~ 0.011	0.15 ~ 0.28
D	0.805±0.005	20.447±0.127
E	0.445±0.005	11.303±0.127
E1	0.555±0.012	14.097±0.305
e	0.050±0.006	1.270±0.152
L	0.033±0.010	0.834±0.25
L1	0.055±0.008	1.397±0.203
y	0.004 Max.	0.1 Max.
θ	0° ~ 10°	0° ~ 10°

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